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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/609,532	06/30/2000	Katsuya Nagashima	Q59989	2000

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Sughrue Mion Zinn MacPeak & Seas PLLC
2100 Pennyslvania Avenue N W
Washington, DC 20037-3213

EXAMINER	
CHANG, EDITH M	
ART UNIT	**PAPER NUMBER**
2634	7

DATE MAILED: 10/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/609,532	NAGASHIMA, KATSUYA	
	Examiner	Art Unit	
	Edith M Chang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim 1 is an apparatus claim, a modulator and its comprised means. In the lines 16-18 of claim 1, "an adapting itself... by using said weighting means and said deciding the order of priority means" is a step of using the apparatus. A single claim which claims both an apparatus and the method step(s) of using the apparatus is indefinite.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7 & 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura (US Patent 5550506) in view of Tsumura (US Patent 5511097).

Regarding **claims 1 & 9**, *except* explicitly using the "feedback loop" term and "adjusting", Tsumura ('506) discloses all subject matter claimed: a demodulator and its methods for a mobile phone (column 1 lines 10-14), which can simultaneously perform operation of improving the demodulation error rate caused by such as noise and external operation being correction after detected, and can reduce the current consumption by restraining the increase of the process time at the simultaneous operation with an external correction circuit after

detected, and can improve the CN ratio (column 1 lines 50-54), comprising: a received error rate improving means (22/23-2 FIG.3) which improves the received error rate by weighting for differences at symbols before (22-1 FIG.3) and after (22-3 FIG.3) a symbol to be demodulated at the present time and applying feedback for symbols; a weighting means(26 & 27 FIG.3, column 4 line 45-column 5 line 6, wherein the MOD and multiplier apply weighting for correction) for applying weighting for correction values after detected of external another loop; a deciding the order of priority means (15 FIG.2/3, column 3 lines 40-46, column 5 lines 35-45) for deciding the order of priority for plural correction values. *However* Tsumura ('097) teaches the "feedback loop" (107 FIG.1) and "an adapting" itself to various radio wave environment and the kinds of noise (column 1 lines 6-14, column 2 lines 20-30 & lines 30-35) by using said weighting means and said deciding the order of priority means. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the Tsumura ('097)'s teachings in Tsumura's demodulator, to specify explicitly the external feedback loop indicated in Tsumura's demodulator ('506 column 4 lines 45-60 where the ideal phase difference based on a tentative demodulated signal from the judging circuit 15) and to adapt itself to achieve the objective of Tsumura ('506)'s demodulator (column 1 lines 10-18, lines 50-54).

Regarding **claims 2 & 10**, Tsumura ('506) discloses a delay circuit and an adder (22/23-2 FIG.3) for obtaining detected phase difference at said symbol point to be demodulated at the present time.

Regarding **claims 3 & 11**, Tsumura ('506) discloses delay circuits and adders for obtaining phase differences at symbol points before (22-1 & 23-1 FIG.3) and after (22-3 & 23-3 FIG.3) said symbol point to be demodulated at the present time.

Regarding **claims 4 & 12**, Tsumura ('506) discloses operation circuits (26 FIG.3) which obtain received quality being difference between each phase difference among symbols obtained at said delay circuits (22-1 FIG.3) and said adders (23-1 FIG.3) and an ideal value (column 4 lines 45-60 wherein the first phase difference is the phase difference obtained at the delay circuit and the adder, and the ideal phase difference is the ideal value, they produce the first phase error that is the output of the operation circuit).

Regarding **claims 5 & 13**, Tsumura ('506) discloses the adders (28 FIG.3) input the received quality obtained at the operation circuits to detected phase value of each of said symbol points before and after said symbol point to be demodulated at the present time by feedback operation.

Regarding **claims 6 & 14**, Tsumura ('506) discloses further comprising: a dividing circuit (15 FIG.3) Which demodulates correctly with using outputs from the adders (14 FIG.3), in case that the detected phase difference at the symbol point to be demodulated includes difference by not detecting phase correctly (column 3 lines 41-47).

Regarding **claims 7 & 15**, Tsumura ('506) discloses the weighting circuits making feedback amounts attenuate (column 5 lines 2-3, wherein the coefficient is a positive value and less than one that attenuate the amounts) in order to avoid divergence of operated results in case that said feedback amounts are large when the adders input the differences by the feedback operation.

5. Claims 8 & 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura (US Patent 5550506) in view of Tsumura (US Patent 5511097), further in view of Saito (US Patent 5260975).

Regarding **claims 8 & 16**. further Saito teaches the logic circuits (65-67 FIG.10) which perform bit expansion at input terminals of the adder (column 12 line 61-column 13 line 5, wherein the latch and the adder perform the bit expansion that the decimal part or the subordinate bits from the latch inputted to an added). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the logic circuit taught by Saito in the Tsumura's ('506)'s demodulator at where the phase data (including the ideal phase difference data inputted to the MOD) directly connected as one of the inputs of the adder to perform bit expansion, to have an excellent bit error rate performance under thermal noises or fading (column 1 lines 5-12 '975).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M Chang whose telephone number is 703-305-3416. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4800.

Edith Chang
October 2, 2003

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600